



Enterprise Computing Solutions - Education Services

OFERTA FORMATIVA

Detalles de contacto

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Hardware Configuration and Definition (HCD) for z/OS

| CÓDIGO: | DURACIÓN: | Precio: |
|---------|-------------------|-----------|
| ES96G | 32 Hours (4 días) | €2,700.00 |

Description

Learn to work with the Hardware Configuration Definition (HCD) function for z/OS, and to plan and initiate dynamic reconfiguration of your zSeries hardware environment. Learn to use the HCD dialogs of z/OS to create an Input/Output (I/O) configuration and dynamically alter the I/O configuration. Learn about the creation of an I/O Configuration Dataset (IOCDs) and various reports that HCD can build. Use a z/OS system to reinforce lecture topics and to practice working with the HCD dialogs. Hands-on lab projects may be done in teams depending on the number of attendees and location.

Objetivos

- Describe new zSeries processor technology
- Code new zSeries processors (z9 to z196)
- Code FICON channels and FICON CTCs
- Code Coupling Facilities (CF) and CF links
- Code cascaded FICON Directors
- Create an IODF work file on a z processor from scratch
- Use CHPID mapping tool to create a validated work IODF
- Use work IODF and create a production IODF
- Perform Dynamic I/O changes on a real z/OS system
- Build a LOADxx parmlib member for initial program load (IPL)
- View configuration graphically
- Create appropriate configuration reports

Público

This course is for people who are responsible for maintaining the I/O configuration contained in the input/output data files (IODFs) and input/output configuration data sets (IOCDs) at their z/OS installation.

Requisitos Previos

You should have:

- A basic knowledge of z/OS and I/O configuration

This knowledge can be developed on the job, or by taking *Fundamental System Skills in z/OS (ES10A)*.

Programa

Day 1

- Welcome
- Unit 1: HCD introduction
- Unit 2: IOCP and MVSCP macro review
- Unit 3: HCD dialog
- Unit 4: LPAR and logical control unit concepts
- Unit 5: OSAs, OSA/ICC and HiperSockets
- Unit 6: Review of zSeries hardware

- Exercise 1: Overview of lab environment
- Exercise 2: HCD familiarity

Day 2

- Unit 7: zSeries I/O architecture: Logical channel subsystems
- Unit 8: Advanced DASD concepts: EAV/PAV and multiple subchannel sets
- Unit 9: FICON, FICON CTCs, and FICON directors
- Exercise 3: Coding a zSeries 2817
- Exercise 4: Adding FICON directors to your configuration (optional)
- Exercise 5: Incremental migration from IOCP deck (optional)

Day 3

- Unit 10: HCD implementation and migration
- Unit 11: IPL and LOADxx member
- Unit 12: Dynamic I/O reconfiguration
- Unit 13: z196 HCD and using CMT
- Exercise 6: Building a LOADxx member
- Exercise 7: Perform dynamic I/O

Day 4

- Unit 14: FICON CTCs for sysplex
- Unit 15: HCD and Parallel Sysplex
- Exercise 8: Coding a 2817 using the CMT
- Exercise 9: Coding CF coupling links
- Exercise 10: Coding sysplex FICON CTCs

Fechas Programadas

A petición. Gracias por [contactarnos](#).

Información Adicional

[Esta formación también está disponible en modalidad presencial. Por favor contáctenos para más información.](#)